

VID4	1	24	+5V
VID3	2	23	VID5
VID2	3	22	RA9
VID1	4	21	GR
VID0	5	20	WNDW'
VC	6	19	RA10
SEGB	7	18	ENVID'
SEGA	8	17	D7
D0	9	16	D6
D1	10	15	D5
D2	11	14	D4
GND	12	13	D3

**Figure 7-8**  
2333 ROM pinouts

+5V	1	16	GND
MDx	2	15	CAS'
R/W'	3	14	MDx
RAS'	4	13	RA1
RA7	5	12	RA4
RA5	6	11	RA3
RA6	7	10	RA2
+5V	8	9	RA0

**Figure 7-9**  
64Kx1 RAM pinouts

$\overline{OE}$	1	18	VSS
I/O1	2	17	I/O4
I/O2	3	16	CAS
WRITE	4	15	I/O3
RAS	5	14	A0
A6	6	13	A1
A5	7	12	A2
A4	8	11	A3
VCC	9	10	A7

**Figure 7-10**  
64Kx4 RAM pinouts

The areas in RAM that are used for the display are accessed both by the 65C02 microprocessor and by the video display circuits. In some computers, this dual access results in addressing conflicts (cycle stealing) that can cause temporary dropouts in the video display. This problem does not occur in the Apple IIe, thanks to the way the microprocessor and the video circuits share the memory.

The memory circuits in the Apple IIe take advantage of the two-phase system clock described earlier in this chapter in the section "65C02 Timing" to interleave the microprocessor memory accesses and the display memory accesses so that they never interfere with each other. The microprocessor reads or writes to RAM only during  $\phi 0$ , and the display circuits read data only during  $\phi 1$ .

### Dynamic-RAM refreshment

The image on a video display is not permanent; it fades rapidly and must be refreshed periodically. To refresh the video display, the Apple IIe reads the data in the active display page and sends it to the display. To prevent visible flicker in the display, and to conform to standard practice for broadcast video, the Apple IIe refreshes the display 60 times per second.

The dynamic RAM devices used in the Apple IIe also need a kind of refresh, because the data is stored in the form of electric charges, which diminish with time and must be replenished every so often. The Apple IIe is designed so that refreshing the display also refreshes the dynamic RAMs. The next few paragraphs explain how this is done.

The job of refreshing the dynamic RAM devices is minimized by the structure of the devices themselves. The individual data cells in each RAM device are arranged in a rectangular array of rows and columns. When the device is addressed, the part of the address that specifies a row is presented first, followed by the address of the column. Splitting information into parts that follow each other in time is called *multiplexing*. Because only half of the address is needed at one time, multiplexing the address reduces the number of pins needed for connecting the RAMs.

Different manufacturers' 64K RAMs have cell arrays of either 128 rows by 512 columns or 256 rows by 256 columns. Only the row portion of the address is used in refreshing the RAMs.