

GND	1	40	H0
GR	2	39	SYNC'
SEGA	3	38	WNDW'
SEGB	4	37	CLRGAT'
VC	5	36	RA10'
80VID'	6	35	RA9'
CASSO	7	34	VID6
SPKR	8	33	VID7
MD7	9	32	KSTRB
AN0	10	31	AKD
AN1	11	30	C0xx
AN2	12	29	A6
AN3	13	28	+5V
R/W'	14	27	Q3
RESET'	15	26	ϕ 0
(n.c.)	16	25	PRAS'
RA0	17	24	RA7
RA1	18	23	RA6
RA2	19	22	RA5
RA3	20	21	RA4

Figure 7-3
IOU pinouts

The 64K dynamic RAMs used in the Apple IIe require a multiplexed address, as described later in this chapter in the section "Dynamic-RAM Timing." The IOU generates this multiplexed address for the data transfers required for display and memory refresh during clock phase 1. The way this address is generated is described later in this chapter in the section "Display Address Mapping." The pinouts and signal descriptions for the IOU are shown in Figure 7-3 and Table 7-7.

Table 7-7
IOU signal descriptions

Pin	Signal	Description
1	GND	Power and signal common
2	GR	Graphics mode enable
3	SEGA	In text mode, works with VC (see pin 5) and SEGB to determine character row address
4	SEGB	In text mode, works with VC (see pin 5) and SEGA; in graphics mode, selects high resolution when low, low resolution when high
5	VC	Display vertical counter bit: in text mode, SEGA, SEGB, and VC determine which of the eight rows of a character's dot pattern to display; in low resolution, selects upper or lower block defined by a byte
6	80VID'	80-column video enable
7	CASSO	Cassette output signal
8	SPKR	Speaker output signal
9	MD7	Internal IOU flags for data bus (bit 7)3
10-13	AN0-AN3	Annunciator outputs
14	R/W'	65C02 read-write control signal
15	RESET'	Power on and reset output
16		(Nothing is connected to this pin.)
17-24	RA0-RA7	Video refresh multiplexed RAM address (phase 1)