

Table 7-11
Display address transformation

H5' V4	V3 H5'	H4 V4	V3 Carry in H3 Augend 1 Addend
S3	S2	S1	S0 Sum

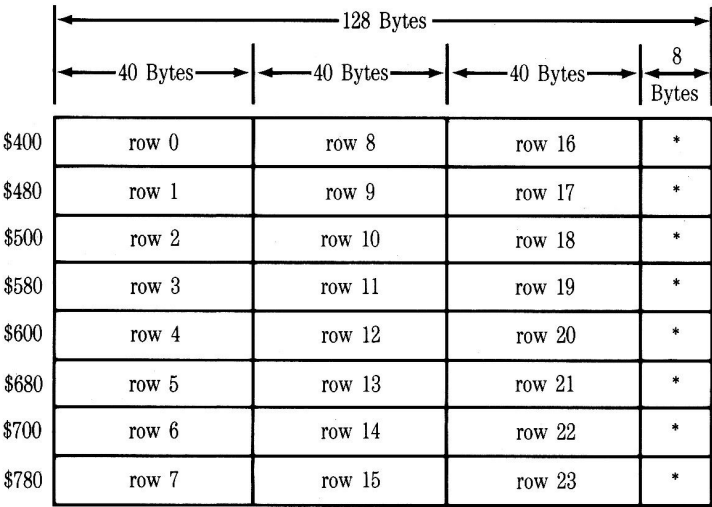


Figure 7-12
40-column text display memory (memory locations marked with an asterisk * are reserved for use by peripheral I/O firmware; refer to the section "Peripheral-Card RAM Space" in Chapter 6)

Table 7-12 shows how the signals from the video counters are assigned to the address lines. H0, H1, and H2 are horizontal-count bits, and V0, V1, and V2 are vertical-count bits. S0, S1, S2 and S3 are the folded address bits described above. Address bits marked with an asterisk (*) are different for different modes: see Table 7-13 and the four subsections under "Video Display Modes."

Table 7-12
Display memory addressing

Memory address bit	Display address bit	Memory address bit	Display address bit
A0	H0	A8	V1
A1	H1	A9	V2
A2	H2	A10	*
A3	S0	A11	*
A4	S1	A12	*
A5	S2	A13	*
A6	S3	A14	*
A7	V0	A15	GND

* For these address bits, see text and Table 7-13.