
Different cycle times

A few instructions on the 65C02 operate in different numbers of cycles than their 65C02 equivalents. These instructions are listed in Table A-1.

Table A-1
Cycle time differences

Instruction/mode	Opcode	6502 cycles	65C02 cycles
ASL Absolute, X	1E	7	6
DEC Absolute, X	DE	7	6
INC Absolute, X	FE	7	6
JMP (Absolute)	6C	5	6
LSR Absolute, X	5E	7	6
ROL Absolute, X	3E	7	6
ROR Absolute, X	7E	7	6

Different instruction results

It is important to note that the BIT instruction when used in immediate mode (opcode \$89) leaves processor status register bits 7 (N) and 6 (V) unchanged on the 65C02. On the 6502, all modes of the BIT instruction have the same effect on the status register: the value of memory bit 7 is placed in status bit 7, and memory bit 6 is placed in status bit 6.

Also note that if the JMP indirect instruction (code \$6C) references an indirect address location that spans a page boundary, the 65C02 fetches the high-order byte of the effective address from the first byte of the next page, while the 6502 fetches it from the first byte of the current page. For example, JMP (\$02FF) gets ADL from location \$02FF on both processors. But on the 65C02, ADH comes from \$0300; on the 6502, ADH comes from \$0200.

Data sheet

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