

## ■ SIGNAL DESCRIPTION

### Address Bus (A0-A15)

A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130pF.

### Clocks ( $\theta_0$ , $\theta_1$ , and $\theta_2$ )

$\theta_0$  is a TTL level input that is used to generate the internal clocks in the 6502. Two full level output clocks are generated by the 6502. The  $\theta_2$  clock output is in phase with  $\theta_0$ . The  $\theta_1$  output pin is 180° out of phase with  $\theta_0$ . (See timing diagram.)

### Data Bus (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF.

### Interrupt Request ( $\overline{IRQ}$ )

This TTL compatible input requests that an interrupt sequence begin within the microprocessor. The  $\overline{IRQ}$  is sampled during  $\theta_2$  operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during  $\theta_1$ . The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further  $\overline{IRQ}$ s may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

### Memory Lock ( $\overline{ML}$ )

In a multiprocessor system, the  $\overline{ML}$  output indicates the need to defer the arbitration of the next bus cycle to ensure the integrity of read-modify-write instructions.  $\overline{ML}$  goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

### Non-Maskable Interrupt ( $\overline{NMI}$ )

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The  $\overline{NMI}$  is sampled during  $\theta_2$ ; the current instruction is completed and the interrupt sequence begins during  $\theta_1$ . The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

Note: Since this interrupt is non-maskable, another  $\overline{NMI}$  can occur before the first is finished. Care should be taken when using  $\overline{NMI}$  to avoid this.

### Ready (RDY)

This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with phase one ( $\theta_1$ ), will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ( $\theta_2$ ) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

### Reset ( $\overline{RES}$ )

This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after VDD reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on  $\overline{RES}$ .

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

### Read/Write ( $R/\overline{W}$ )

This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location.

### Set Overflow ( $\overline{SO}$ )

A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of  $\theta_1$ .

### Synchronize (SYNC)

This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during  $\theta_1$  of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the  $\theta_1$  clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.