

The data for each row of characters are read eight times, once for each of the eight lines of dots making up the row of characters. The data bits are sent to the character generator ROM along with VA, VB, and VC, the low-order bits from the vertical counter. For each character being displayed, the character generator ROM puts out one of eight stored bit patterns selected by the three-bit number made up of VA, VB, and VC.

The bit patterns from the character generator ROM are loaded into the 74166 parallel-to-serial shift register and output as a serial bit stream that goes to the video output circuit. The shift register is controlled by signals named LDPS' (for load parallel-to-serial shifter) and VID7M (for video 7 MHz). In 40-column mode, LDPS' strobes the output of the character generator ROM into the shift register once each microsecond, and bits are sent to the screen at a 7 MHz rate.

The addressing for the 80-column display is exactly the same as for the 40-column display: the 40 columns of display memory on the 80-column card are addressed in parallel with the 40 columns in main memory. The data from these two memories reach the video data bus (lines VID0-VID7) via separate 74LS374 three-state buffers. These buffers are loaded simultaneously, but their outputs are sent to the character generator ROM alternately by $\phi 0$ and $\phi 1$. In 80-column mode, LDPS' loads data from the character generator ROM into the shift register twice during each microsecond, once during $\phi 0$ and once during $\phi 1$, and bits are sent to the screen at a 14 MHz rate. Figures 7-13a and 7-13b show the video timing signals.