

**Table 7-13**  
Memory address bits for display modes

Address bit	Display modes	
	Text and low resolution	High resolution and double high resolution
A10	80STORE+PAGE2'	VA
A11	80STORE'.PAGE2	VB
A12	0	VC
A13	0	80STORE+PAGE2'
A14	0	80STOREv'.PAGE2

*Note:* Period (.) means logical AND; prime (') means logical NOT.

## Video display modes

The different display modes all use the address-mapping scheme described in the preceding section, but they use different-sized memory areas in different locations. The next four sections describe the addressing schemes and the methods of generating the actual video signals for the different display modes.

### Text displays

The text and low-resolution graphics pages begin at memory locations \$0400 and \$0800. Table 7-13 shows how the display-mode signals control the address bits to produce these addresses. Address bits A10 and A11 are controlled by the settings of PG2 and 80STORE, which are set by the display-page and 80-column-video soft switches. Address bits A12, A13, and A14 are set to 0. Notice that 80STORE active inhibits PG2: there is only one display page in 80-column mode.

The bit patterns used for generating the different characters are stored in a 32K ROM. The low-order six bits of each data byte reach the character generator ROM directly, via the video data bus VID0–VID5. The two high-order bits are modified by the IOU to select between the primary and alternate character sets and are sent to the character generator ROM on lines RA9 and RA10.