

GND	1	40	A1
A0	2	39	A2
$\phi 0$	3	38	A3
Q3	4	37	A4
PRAS'	5	36	A5
RA0	6	35	A6
RA1	7	34	A7
RA2	8	33	A8
RA3	9	32	A9
RA4	10	31	A10
RA5	11	30	A11
RA6	12	29	A12
RA7	13	28	A13
R/W'	14	27	A14
INH'	15	26	A15
DMA'	16	25	+5V
EN80'	17	24	Cxxx
KBD'	18	23	RAMEN'
ROMEN2'	19	22	R/W' 245
ROMEN1'	20	21	MD7

Figure 7-2
MMU pinouts

Table 7-6
MMU signal descriptions

Pin	Signal	Description
1	GND	Power and signal common
2	A0	65C02 address input
3	$\phi 0$	Clock phase 0 input
4	Q3	Timing signal input
5	PRAS'	Memory row-address strobe
6–13	RA0–RA7	Multiplexed address output
14	R/W'	65C02 read-write control signal
15	INH'	Inhibits main memory (tied to +5V)
16	DMA'	Controls data bus for DMA transfers
17	EN80'	Enables auxiliary RAM
18	KBD'	Enables keyboard data bits 0–6
19	ROMEN2'	Enables ROM (tied to ROMEN1')
20	ROMEN1'	Enables ROM (tied to ROMEN2')
21	MD7	State of MMU flags on data bus bit 7
22	RW' 245	Controls 74LS245 data-bus buffer
23	RAMEN'	Enables main RAM
24	Cxxx	Enables peripheral-card memory
25	+5V	Power
26–40	A15–A1	65C02 address input

The Input/Output Unit

The circuitry inside the Input/Output Unit (IOU) implements the following soft switches, all described in Chapter 2 in this manual:

- ☐ Page 2 display (PAGE2)
- ☐ high-resolution mode (HIRES)
- ☐ text mode (TEXT)
- ☐ mixed mode (MIXED)
- ☐ 80-column display (80COL)
- ☐ text display mode select (ALTCHAR)
- ☐ any-key-down
- ☐ annunciators
- ☐ vertical blanking (VBL)