

The IOU performs an addition that reduces the five significant count bits to four new signals called S0, S1, S2, and S3, where S stands for sum. Figure 7-12 is a diagram showing the addition in binary form, with V3 appearing as the carry in and H5 appearing as its complement H5'. A constant value of 1 appears as the low-order bit of the addend. The carry bit generated with the sum is not used.

If this transformation seems obscure, try it with actual values. For example, for the upper-left corner of the display, the vertical count is 0 and the horizontal count is 24: H0, H1, H2, and H5 are 0's, and H3, and H4 are 1's. The value of the sum is 0, so the memory location for the first character on the display is the first location in the display page, as you might expect.

Horizontal bits H0, H1, and H2 and sum bits S0, S1, and S2 make up the transformed horizontal address (A0 through A6 in Table 7-12). As the horizontal count increases from 24 to 63, the value of the sum (S3 S2 S1 S0) increases from 0 to 4 and the transformed address goes from 0 to 39, relative to the beginning of the display page.

The low-order three bits of the vertical row counter are V0, V1, and V2. These bits control address bits A7, A8, and A9, as shown in Table 7-12, so that rows 0 through 7 start on 127-byte boundaries. When the vertical row counter reaches 8, then V0, V1, and V2 are 0 again, and V3 changes to 1. If you do the addition in Table 7-11 with H equal to 24 (the horizontal count for the first column displayed) and V equal to 8, the sum is 5 and the horizontal address is 40: the first character in row 8 is stored in the memory location 40 bytes from the beginning of the display page.

Figure 7-12 shows how groups of 3 40-character rows are stored in blocks of 120 contiguous bytes starting on 127-byte address boundaries. This diagram is another way of describing the display mapping shown in Figure 2-6. Notice that the 3 rows in each block of 120 bytes are not adjacent on the display.