

## The peripheral address bus

The microprocessor's address bus is buffered by two 74LS244 octal three-state buffers. These buffers, along with a buffer in the microprocessor's R/W' line, are enabled by a signal derived from the DMA' daisy chain on the expansion slots. Pulling the peripheral line DMA' low disables the address and R/W' buffers so that peripheral DMA circuitry can control the address bus. The DMA address and R/W' signals supplied by a peripheral card must be stable all during  $\phi 0$  of the instruction cycle, as shown in Figure 7-14.

Another signal that can be used to disable normal operation of the Apple IIe is INH'. Pulling INH' low disables all of the memory in the Apple IIe except the part in the I/O space from \$C000 to \$CFFF. A peripheral card that uses either INH' or DMA' must observe proper timing; in order to disable RAM and ROM cleanly, the disabling signal must be stable all during  $\phi 0$  of the instruction cycle (refer to the timing diagram in Figure 7-14).

The peripheral devices should use I/O SELECT' and DEVICE SELECT' as enables. Most peripheral ICs require their enable signals to be present for a certain length of time before data is strobed into or out of the device. Remember that I/O SELECT' and DEVICE SELECT' are only asserted during  $\phi 0$  high.

## The peripheral data bus

The Apple IIe has two versions of the microprocessor data bus: an internal bus, MD0-MD7, connected directly to the microprocessor; and an external bus, D0-D7, driven by a 74LS245 octal bidirectional bus buffer. The 65C02 is fabricated with MOS circuitry, so it can drive capacitive loads of up to about 130 pF. If peripheral cards are installed in all seven slots, the loading on the data bus can be as high as 500 pF, so the 74LS245 drives the data bus for the peripheral cards. The same argument applies if you use MOS devices on peripheral cards: they don't have enough drive for the fully loaded bus, so you should add buffers.