

The branch table locations that Pascal 1.1 firmware protocol uses are as follows:

Address	Contains
\$Cs0D	Initialization routine offset (required)
\$Cs0E	Read routine offset (required)
\$Cs0F	Write routine offset (required)
\$Cs10	Status routine offset (required)
\$Cs11	\$00 if optional offsets follow; nonzero if not
\$Cs12	Control routine offset (optional)
\$Cs13	Interrupt handling routine offset (optional)

Notice that \$Cs11 contains \$00 only if the control and interrupt handling routines are supported by the firmware. (For example, the SSC does not support these two routines, and so location \$Cs11 contains a nonzero firmware instruction.) Apple II Pascal 1.0 and 1.1 do not support control and interrupt requests, but such requests are implemented in Pascal 1.2 and later versions and in ProDOS.

Table 6-7 gives the entry point addresses and the contents of the 65C02 registers on entry to and on exit from Pascal 1.1 I/O routines.

Table 6-7
I/O routine offsets and registers under Pascal 1.1 protocol

Address	Offset for	X register	Y register	A register
\$Cs0D	Initialization			
	On entry	\$Cs	\$s0	
	On exit	Error code	(unchanged)	(unchanged)
\$Cs0E	Read			
	On entry	\$Cs	\$s0	
	On exit	Error code	(unchanged)	Character read
\$Cs0F	Write			
	On entry	\$Cs	\$s0	Char. to write
	On exit	Error code	(unchanged)	(unchanged)
\$Cs10	Status			
	On entry	\$Cs	\$s0	Request (0 or 1)
	On exit	Error code	(changed)	(unchanged)