

The EN80' enable signal is controlled by the 80STORE soft switch described in Chapter 4. Data is sent to the auxiliary memory via the internal data bus MD0–MD7; the data is transferred to the video generator via the video data bus VID0–VID7.

Table 7-21
Auxiliary slot signals

Pin	Signal	Description
1	3.58M	3.58 MHz video color reference signal. This line can drive two LS TTL loads.
2	VID7M	Clocks the video dots out of the 74166 parallel-to-serial shift register. This line can drive two LS TTL loads.
3	SYNC'	Video horizontal and vertical sync signal. This line can drive two LS TTL loads.
4	PRAS'	Multiplexed RAM row-address strobe. This line can drive two LS TTL loads.
5	VC	Third low-order vertical-counter bit. This line can drive two LS TTL loads.
6	C07X'	Hand-control reset signal. This line can drive two LS TTL loads.
7	WNDW'	Video nonblank window. This line can drive two LS TTL loads.
8	SEGA	First low-order vertical counter bit. This line can drive two LS TTL loads.
51,10,49, 48,13,14, 46,9	RA0–RA7	Multiplexed RAM-address bus. This line can drive two LS TTL loads.
11,12	ROMEN1, ROMEN2	Enable signals for the ROMs on main circuit board.
44,43,40, 39,21,20, 17,16	MD0–MD7	Internal (unbuffered) data bus. This line can drive two LS TTL loads.