

Chapter 7 Hardware Implementation 157

| | | |
|--------------|---|-----|
| Figure 7-1 | 65C02 timing signals | 163 |
| Figure 7-2 | MMU pinouts | 165 |
| Figure 7-3 | IOU pinouts | 166 |
| Figure 7-4 | PAL pinouts | 167 |
| Figure 7-5 | 2364 ROM pinouts | 168 |
| Figure 7-6 | 23128 ROM pinouts | 169 |
| Figure 7-7 | 2316 ROM pinouts | 169 |
| Figure 7-8 | 2333 ROM pinouts | 170 |
| Figure 7-9 | 64Kx1 RAM pinouts | 170 |
| Figure 7-10 | 64Kx4 RAM pinouts | 170 |
| Figure 7-11 | RAM timing signals | 172 |
| Figure 7-12 | 40-column text display memory | 177 |
| Figure 7-13a | 7 MHz video timing signals | 180 |
| Figure 7-13b | 14 MHz video timing signals | 181 |
| Figure 7-14 | Peripheral-signal timing | 194 |
| Figure 7-15 | Original and enhanced I/O schematic diagram | 201 |
| Figure 7-16 | Extended keyboard I/O schematic diagram | 205 |
| Table 7-1 | Summary of environmental specifications | 158 |
| Table 7-2 | Power supply specifications | 159 |
| Table 7-3 | Power connector signal specifications | 160 |
| Table 7-4 | 65C02 microprocessor specifications | 161 |
| Table 7-5 | 65C02 timing signal descriptions | 163 |
| Table 7-6 | MMU signal descriptions | 165 |
| Table 7-7 | IOU signal descriptions | 166 |
| Table 7-8 | PAL signal descriptions | 167 |
| Table 7-9 | RAM address multiplexing | 171 |
| Table 7-10 | RAM timing signal descriptions | 172 |
| Table 7-11 | Display address transformation | 177 |
| Table 7-12 | Display memory addressing | 177 |
| Table 7-13 | Memory address bits for display modes | 178 |
| Table 7-14 | Character-generator control signals | 181 |
| Table 7-15 | Internal video connector signals | 186 |
| Table 7-16 | Keyboard connector signals | 187 |
| Table 7-17 | Keypad connector signals | 188 |
| Table 7-18 | Speaker connector signals | 189 |
| Table 7-19 | Game I/O connector signals | 190 |
| Table 7-20 | Expansion slot signals | 194 |
| Table 7-21 | Auxiliary slot signals | 198 |